REMARKS

An Excess Claim Fee Payment Letter is attached hereto for one (1) excess independent claim.

Claims 1-21 and 36-38 are all of the claims pending in the application. New claims 36-28 have been added to more completely define the invention.

Claim 1-21 stand rejected on prior art grounds, and claims 1-17 stand rejected under 35 U.S.C. §112, second paragraph, as being "indefinite". Non-elected claims 22-35 have been canceled above.

Applicant gratefully acknowledges the Examiner's indication that claims 6, 11, and 13 would be allowable if rewritten in independent form. Claims 6 and 11 have been rewritten accordingly to place each of claims 6, 11, and 13 in condition for immediate allowance.

With respect to the prior art rejections, claims 1-4, 7-8, 12, and 14-18 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Linn et al. (U.S. Patent No. 5,387,555). Claim 5 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Linn et al. in view of Maiti et al. (U.S. Patent No. 6,049,114). Claims 9-10 and 19-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Linn et al. in view of Chan et al. (U.S. Patent No. 6,057,212.

These rejections are respectfully traversed in view of the following discussion.

Attached hereto is a marked-up version of the changes made to the claims by the present Amendment. The attached page(s) is captioned "**Version with Markings to Show Changes Made**".

It is noted that the claim amendments herein are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims, or for any statutory requirements of patentability.

Further, it is noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed (e.g., see independent claim 1), is directed to a method (and resultant structure) of forming a semiconductor device, which includes forming a metal-back-gate over a substrate and a metal back-gate, forming a passivation layer on the metal back-gate to prevent the metal back-gate from reacting with radical species, and providing an intermediate gluing layer between the substrate and the metal back-gate to enhance adhesion between the substrate and the metal back-gate. Such features allow the problems of the conventional methods to be overcome.

That is, laminating a thin metal layer (e.g., tungsten (W)) between silicon-based materials such as a gate oxide and a buried oxide is a key step to making substrates for double-gate devices with a metal back-gate. Because of its flexibility with all kinds of materials, even if the materials are polycrystalline, amorphous, or single crystalline but with very different lattice mismatch, wafer bonding is a promising approach to make this multilayer structure.

However, for the bonding process, after the room-temperature joining step, a thermal treatment at 1100 °C is commonly used to enhance the bonding strength. Due to the weak adhesion at the interface between metals and, for example, silicon oxide as a result of their chemical and physical incompatibility such as thermal mismatch, the stacked layers are very likely to disintegrate during the high temperature bonding anneal in the form of delamination at weak interfaces.

A key feature of the method of the present invention is to use an intermediate "gluing" layer to enhance adhesion between multi-layers especially two layers with very different chemical and physical properties.

With the above and other unique and unobvious aspects of the present invention, making substrates for double-gate devices with a metal back-gate can be performed including using wafer bonding and despite after the room-temperature joining step, a thermal treatment at 1100°C is used to enhance the bonding strength.

That is, even with chemical and physical incompatibility of layers, the stacked layers are not likely to disintegrate during the high temperature bonding anneal, and delamination will not occur at the interfaces.

Thus, the present invention resolves the above-mentioned and other problems of delamination between, for example, W and low temperature oxide (LTO) during bonding anneal by improving the adhesion between these two incompatible materials with several innovative processes.

None of the cited references, either alone or in combination, teaches or suggests such a combination of features.

II. THE 35 U.S.C. §112, SECOND PARAGRAPH, REJECTION

Claims 1-17 stand rejected under 35 U.S.C. §112, second paragraph, as being "indefinite". Claims 1-17 have been amended in a manner believed fully responsive to all points raised by the Examiner.

However, regarding claim 1, Applicant submits that this claim is believed to be clear and definite to one of ordinary skill in the art. It is noted that, contrary to the Examiner's indications on page 2 of the Office Action, the back-gate is defined as being formed "over" the substrate in claim 1. Thus, the language of claim 1 is believed to be consistent with the remaining claims, and clear and sufficiently definite to allow one of ordinary skill in the art to know the metes and bounds of the claim.

In view of the foregoing, reconsideration and withdrawal of this rejection are respectfully requested.

III. THE PRIOR ART REJECTIONS

As described below, the claimed invention differs from each of the cited references, either alone or in combination, by the recitation of the intermediate "gluing" layer to enhance adhesion between multi-layers especially two layers with very different chemical and physical properties.

As mentioned above, the present invention resolves the above-mentioned and other problems of delamination between metals and , for example, a low temperature oxide (LTO) during bonding anneal by improving the adhesion between two incompatible materials with several innovative processes.

Thus, the claimed invention is patentable over all of the prior art of record, as

discussed below for the record.

A. The Linn et al. Reference

Linn et al. discloses a bonded wafer processing with metal silicidation. However, Linn et al. is completely irrelevant to the claimed invention.

First, even if Linn et al. bears some superficial similarities with the claimed invention, the principle of operation and fabrication of Linn et al. is completely different from the claimed invention, and thus Linn et al. fails to teach or suggest the claimed invention.

Indeed, in the invention defined by independent claim 1, an intermediate gluing layer is provided on the passivation layer to enhance adhesion between the metal back-gate and the substrate.

In contrast, in Figures 5A-5B of Linn et al., a method of bonded wafer processing is shown in which a first structure is formed including a substrate 512 having an oxide 513 formed thereon, and a polysilicon layer is formed on the oxide 513. An oxidizer 505 is formed on the polysilicon 514. Thereafter, this first structure is bonded to a second structure. The second structure includes a silicon device wafer 502, an oxide 506 formed on the silicon device wafer 502, a polysilicon 517 formed on the oxide 506, and a tungsten layer is formed on the polysilicon 517.

The resultant structure is shown in Figure 5b and includes substrate 512, oxide 513, SiOxNy 519, WSi 515, oxide 506, and silicon device wafer 502.

The Examiner indicates that Figure 5A-5B illustrate a passivation layer on the metal back-gate and an intermediate glueing layer on the passivation layer, and that the intermediate gluing layer comprises a silicon layer. However, Applicant respectfully disagrees.

Presumably, the Examiner is relying on layer 517 as the "intermediate gluing layer" of the claimed invention. However, this is erroneous. That is, the intermediate gluing layer of the claimed invention is for enhancing adhesion between the metal back-gate and the substrate. The polysilicon layer 517 performs no such function, nor is such disclosed or suggested by Linn et al.

Indeed, nowhere is there any mention within the four corners of Linn et al. that the polysilicon layer is 517 is an intermediate gluing layer provided on a passivation layer for

enhancing the adhesion between the tungsten layer and the substrate of Linn et al.

Thus, Linn et al. fails to teach or suggest "*[a] method of forming a semiconductor substrate, comprising:*

forming a metal back-gate over a substrate;

forming a passivation layer on the metal back-gate to prevent the metal back-gate from reacting with radical species; and

providing an intermediate gluing layer on said passivation layer to enhance adhesion between said metal back-gate and said substrate", as defined by independent claim 1.

Independent claim 18 is patentable for somewhat similar reasons in that no passivation layer(if any) formed in Linn et al. is for enhancing adhesion between the substrate and the metal back-gate.

Therefore, Linn et al. fails to anticipate or, for that matter, render obvious the claimed invention defined by claims 1-4, 7-8, 12, and 14-18.

B. The Secondary References to Maiti et al. and Chan et al.

Regarding the rejection of claim 5 and the rejection of claims 9-10 and 19-21, the Examiner additionally relies on Maiti and Chan et al., respectively, for making up for the deficiencies of Linn et al. Applicant respectfully disagrees.

First, Applicant submits that one of ordinary skill in the art would not have made the Examiner's urged combination of references. Indeed, the Examiner provides no reason for making the combination other than a general assertion that it would have been obvious to combine Linn et al. and Maiti since "Maiti et al. teach that this process is interchangeable with PVD", and that it would have been obvious to combine Linn et al. and Chan et al. since "Linn et al. discloses a silicon substrate and Chan et al. teaches a possible substrate". Thus, the Examiner has failed to make out a prima facie case of obviousness.

Moreover, this "reason" is completely irrelevant to the claimed invention and has nothing to do with what the invention is directed, let alone the solution that it offers or, for that matter, the problems of Linn et al., Maiti et al., and Chan et al. Quite simply, each of Linn et al., Maiti et al. and Chan et al. is directed to completely different problems, and offer completely different solutions to these problems.

Indeed, Maiti et al. has merely attempted to replacing polysilicon gates with metal containing gates to overcome the problems associated with poly depletion, whereas Chan is directed to controlling the flow of electrons by the gate and independent of drain voltage, and more specifically attempting to attach an insulator layer to a metal in atomically intimate contact and with a negligible interface reaction.

Thus, there is no reason or motivation to modify Linn's method with Maiti or Chan et la., as compared to another type of method. It is clear that there would have been no reason or motivation to make the Examiner's urged combination, absent hindsight.

Secondly, even if the references would have been combined, the claimed invention would still not have been produced.

That is, even if Maiti teaches that PVD and CVD are interchangeable, the above-mentioned deficiencies of Linn et al. are still not cured by Maiti et al. or Chan et al.

Thus, there is no teaching or suggestion of "*providing an intermediate gluing layer on said passivation layer to enhance adhesion between said metal back-gate and said substrate*", as defined by independent claim 1.

Hence, claims 5, 9-10, and 17-19 would not have been rendered obvious by the Examiner's urged combinations of Linn et al. in view of either of Maiti et al. or Chan et al.

Hence, turning to the clear language of the claims, there is no teaching or suggestion of "*[a]" method of forming a semiconductor substrate, comprising:*

forming a metal back-gate over a substrate;

forming a passivation layer on the metal back-gate to prevent the metal back-gate from reacting with radical species; and

providing an intermediate gluing layer on said passivation layer to enhance adhesion between said metal back-gate and said substrate (emphasis Applicant's), as defined by independent claim 1.

Further, there is no teaching or suggestion of "*[a] method of forming a semiconductor substrate, comprising:*

forming a metal back-gate over a substrate; and

providing a passivation layer between said substrate and said metal back-gate to enhance adhesion therebetween (emphasis Applicant's), as defined by independent claim 18.

Finally, there is no teaching or suggestion of "*[a] method of forming a semiconductor substrate, comprising:*

growing a gate oxide on a silicon-on-insulator (SOI) material;

depositing a refractory metal onto said gate oxide; and

forming a passivation layer on said refractory metal" (emphasis Applicant's), as defined by independent claim 19.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

Further, the other prior art of record has been reviewed, but it too even in combination with Linn et la., Maiti et al., and Chan et al. fails to teach or suggest the claimed invention.

III. FORMAL MATTERS AND CONCLUSION

Regarding the Examiner's objection to the drawings, submitted herewith is a proposed drawing correction to label passivation layer 305 in Figure 3A. It is noted that the metal layer 303 is passivated to form a passivation layer 305. Reconsideration and withdrawal of this objection are respectfully requested.

Claim 6 has been amended to overcome the Examiner's objection thereto.

A Substitute Specification is attached hereto to insert the application data on page 7, line 20 and to provide a margin for the Examiner's convenience. No new matter has been added.

In view of the foregoing, Applicant submits that claims 1-21 and 36-38, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

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Sean M. McGinn, Esq.
Reg. No. 34,386

McGinn & Gibb, PLLC
8321 Old Courthouse Rd. Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer No. 21254

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

2. (Amended) The method of claim 1, wherein said intermediate gluing layer comprises one of a-Si, Si_3N_4 and a combined layer of a-Si and Si_3N_4 .

4. (Amended) The method of claim 3, wherein said depositing of said W comprises a [plasma] physical vapor deposition (PVD) of W.

6. (Amended) [The method of claim 1] A method of forming a semiconductor substrate, comprising:

forming a metal back-gate over a substrate;

forming a passivation layer on the metal back-gate to prevent the metal back-gate from reacting with radical species; and

providing an intermediate gluing layer on said passivation layer to enhance adhesion between said metal back-gate and said substrate,

wherein said forming of said metal back-gate comprises:

conducting UHV desorption of native oxide on W under a pressure of 10^{-9} torr at 750°C for 5 minutes;

forming a monolayer of W-Si silicide at 625°C for 1.5 [min. reaction with] minutes using SiH_4 such that a bare W surface reacts with Si to form a monolayer of W-Si; and

performing nitridation of W-Si at 750°C for 30 [min.] minutes with NH_3 and reacting active NH_2 with W-Si to form W-Si-N.

12. (Amended) The method of claim 1, wherein a multilayer stack is formed on said substrate, wherein said substrate with [a] said multilayer stack is bonded to a silicon substrate and annealed to strengthen the bond across the bonding interface.

16. (Amended) The method of claim 15, wherein annealing conditions including any of a ramp-up rate, a ramp-down rate, a [stablization] stabilization temperature, and a stabilization temperature time are optimized to minimize stress induced by thermal mismatch of different materials of said metal back-gate, said substrate, said passivation layer and said intermediate gluing layer.

17. (Amended) The method of claim 1, wherein said intermediate gluing layer comprises a Si-based intermediate layer.